

Combining static priority and weighted round-robin like packet scheduling in AFDX for incremental certification and mixed criticality support

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Abstract:

Avionics Full Duplex (AFDX) is an aeronautic-specific switched Ethernet technology that provides data exchanges among avionics sub-systems with bounded latencies, without requiring the sub-systems to share a common global clock like in TDMA networks. These predictable latencies can be achieved because the workload submitted to the network by each sub-system is upper bounded and known in advance, and because the standard enforces appropriate switching mechanisms within the communication switches. In particular, the packets waiting to be sent on an output port of a communication switch are to be stored in a FIFO queue or in distinct queues depending on their priorities (high or low). The use of priorities (static priorities on a per-flow basis) actually helps meeting more stringent latencies for the most critical data flows than what would be feasible with FIFO queues alone. However, scheduling with priorities in itself does not provide a solution to the issue of incremental certification. Indeed adding a single data stream may have an impact on all the other streams that are transmitted, which requires re-computing the upper bounds on the latencies, and, possibly, involves reconfiguring the communication parameters throughout the whole system.

In this paper, we study the combined use of static priority and Deficit Round Robin (DRR) to schedule the transmissions of the packets on the output links of the AFDX switches. DRR is a low-complexity weighted round-robin like policy which allows the flows to share the available bandwidth according to some pre-defined percentages. Practically, DRR guarantees that a flow or a set of flows will be provided at run-time at least the share of bandwidth that has been allocated to them. If some spare bandwidth is provisioned for future use, it becomes possible to add new data flows to an existing system without any impact on the real-time performances of the pre-existing flows. Importantly, this opens the doors to incremental certification. Among the numerous variants of Round-Robin, DRR is an appealing policy in the avionics context because it is predictable in terms of worst-case latencies [1,2] and the associated run-time overhead within the switches is contained (there are $O(1)$ implementations [3]). Besides, DRR does not require any changes in the AFDX frame format or at the end-systems level (e.g. communication stack): only the switches need to implement new mechanisms and offer additional configuration parameters. However, AFDX is often intended to support traffic with mixed-criticalities, specifically in terms of timing requirements, which cannot be achieved with

DRR alone since increasing the bandwidth share for a flow or a set of flows does not decrease the worst-case latency. As we will explain, this can be best achieved by using priorities that reflects the criticalities of the flows.

The first objective of the paper is to study how DRR and prioritized scheduling can be best used in a combined manner, in order to support both incremental certification and data flows with mixed timing criticalities. This question will be discussed considering the evolutions that can be foreseen in terms of technology (e.g., Gbit/s switches) and traffic characteristics (e.g., increasing low-criticality entertainment-related traffic).

The second objective and core contribution of the paper is to provide a quantitative assessment on realistic case-studies[4] that supports our proposal and identifies its range of applicability. Specifically, the latency overhead with DRR (wrt to priority scheduling) will be evaluated and it will be shown that, be it at 100Mbit/s or 1Gbit/s, DDR alone is not suited for the most stringent timing constraints. Then, it will be shown that, taking advantage of the increasing bandwidth, combining static priority and DRR provides a practical and efficient solution for next generation avionics systems with mixed-criticality traffic and the need for incremental certification.

1 References

[1] M. Boyer, G. Stea, W. Mangoua Sofack, "Deficit Round Robin with network calculus," 6th International Conference on Performance Evaluation Methodologies and Tools (VALUETOOLS 2012), pp.138-147, 9-12 Oct. 2012.

[2] H. Yu, L. Xue, "Scheduling design and analysis for end-to-end heterogeneous flows in an avionics network" INFOCOM 2011, pp2417-2425, 2010.

[3] L. Lenzini, E. Mingozzi, G. Stea, "Aliquem: a novel DRR implementation to achieve better latency and fairness at $O(1)$ complexity," Tenth IEEE International Workshop on Quality of Service, pp. 77- 86, 2002.

[4] M. Boyer, N. Navet, M. Fumey, "Experimental assessment of timing verification techniques for AFDX", Embedded Real-Time Software and Systems (ERTS 2012), Toulouse, France, February 1-3, 2012.