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A feasibility study on large-scale TASEP simulations using cutting-edge vector processors

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The totally asymmetric simple exclusion process (TASEP) has been extensively studied in the field of non-equilibrium statistical mechanics [1]. By employing the simple characteristic that a particle hops in a single direction with the constraint of volume exclusion effect, the TASEP has been applied to many practical problems. The importance of carrying out large-scale TASEP simulations has been recognized. However, the parallel computing of TASEP is quite challenging because it has complex conditional branches and deeply nested loops. In additions, the amount of memory access is much greater than that of floating-point operation; existing accelerators such as GPU (Graphics Processing Units) are not suitable for TASEP simulations.

The NEC SX-Aurora TSUBASA is a cutting-edge vector processor which comprises 1.4 GHz 8-core with 150 GB/s average memory bandwidth and delivers more than 2.15 TeraFLOPS peak performance, and 1.20 TB/s memory bandwidth in whole system [2]. The SX-Aurora TSUBASA is considered to be compatible with TASEP algorithm because of high memory bandwidth. There are expectations that it becomes the breakthrough of large-scale CA (cellular automaton) based simulations including TASEP.

In this study, we investigate the computational performance of TASEP simulations on the SX-Aurora TSUBASA A300-2 server. The performance scalability of a test case TASEP simulation is examined on the system. For comparisons, the flops (floating-point operations per second) and scalability for stencil-based simulations of three-dimensional diffusion equations are also investigated. A simulation analysis of spot assignments in airport ground transportations using TASEP is successfully demonstrated. To summarize, we discuss the applicability of the SX-Aurora system to large-scale TASEP simulations.

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